AMENDMENTS TO THE CLAIMS

Claim Amendments and Status:

1. (canceled).

2. (currently amended) An ~~The~~ asynchronous pulse logic circuit ~~of claim 1, further~~ comprising:

a first pulse generating component for generating a sending pulse;

a first converting component for catching and holding said sending pulse and converting said sending pulses to a first level voltage connected to said first pulse generating component;

a second pulse generating component for generating a resetting pulse;

a second converting component for converting said resetting pulse to a second level voltage connected to said second pulse generating component;

a checking component for ensuring no old output is still pending;

an N-input component connected to said first pulse generating component; and

an N-output component connected to said first converting component whereby a STAPL left-right buffer is formed.

3. (currently amended) An ~~The~~ asynchronous pulse logic circuit ~~of claim 1, further~~ comprising:

a first pulse generating component for generating a sending pulse;

a first converting component for catching and holding said sending pulse and converting said sending pulses to a first level voltage connected to said first pulse generating component; and

a checking component for ensuring no old output is still pending whereby said checking component is connected to said first pulse generating component and said first converting component to form a first input-output block.

4. (original) The asynchronous pulse logic circuit of claim 3 further comprises:

a plurality of said input-output blocks.

5. (previously presented) The asynchronous pulse logic circuit of claim 4 further comprises:

an input-clearing block comprising a second converting component for converting pulses.

6. (previously presented) The asynchronous pulse logic circuit of claim 5 further comprises:

an acknowledgment block comprising a second pulse generating component for generating a resetting pulse.

7. (previously presented) The asynchronous pulse logic circuit of claim 6 further comprises:

a conditions block whereby said second pulse generating component is controlled by said conditions block to conditionally reset each of said plurality of input-output blocks and input clearing block.

8. (previously presented) The asynchronous pulse logic circuit of claim 7 wherein said conditions block further comprises:

a third pulse generating component for generating a sending pulse; and

a third converting component for converting said sending pulses to said first level voltage connected to said third pulse generating component.

9. (currently amended) The asynchronous pulse logic circuit of claim ~~1~~ 2 wherein said first converting component is modified to store states.

10. (previously presented) The asynchronous pulse logic circuit of claim 9 further comprises:

an updating component comprising an interlock component wherein an updating pulse is generated to update the input state in said first pulse generating component, whereby a state-storing circuit is formed.

11. (currently amended) The asynchronous pulse generating circuit of claim ~~1~~ 2 further comprises:

an arbiter-filter, wherein~~; and~~

~~a checking component for ensuring no old output is still pending whereby~~ said checking component and said arbiter-filter are connected to said first pulse generating component and said first converting component to form a STAPL arbiter.

12. (previously presented) The asynchronous pulse generating circuit of claim

11 wherein said first pulse generating component generates a reset pulse for the input.

13. (previously presented) The asynchronous pulse generating circuit of claim 11 wherein said first pulse generating component further comprises an interlock component.

14. (previously presented) The asynchronous pulse generating circuit of claim 2 further comprises:

a QDI buffer connected to said STAPL left-right buffer whereby an STAPL-to-QDI converter is formed.

15. (previously presented) The asynchronous pulse generating circuit of claim 2 further comprises:

a QDI buffer connected to said STAPL left-right buffer whereby an QDI-to-STAPL converter is formed.

16. (previously presented) An asynchronous pulse logic circuit comprising:

a first pulse generating component for generating a sending pulse;

a first converting component for converting pulses to a first level voltage connected to said first pulse generating component;

a second pulse generating component for generating a resetting pulse;

a second converting component for converting pulses to a second level voltage connected to said second pulse generating component;

a checking component for ensuring no old output is still pending;

an N-input component connected to said first pulse generating component; and

an N-output component connected to said first converting component whereby a STAPL left-right buffer is formed.

17. (currently amended)The asynchronous pulse logic circuit of claim 16 wherein ~~further comprises:~~

~~a checking component for ensuring no old output is still pending whereby~~ said checking component is connected to said first pulse generating component and said first converting component to form a first input-output block.

18. (previously presented) The asynchronous pulse logic circuit of claim 17 further comprises:

a plurality of said input-output blocks.

19. (previously presented) The asynchronous pulse logic circuit of claim 18 further comprises:

an input-clearing block comprising a second converting component for converting pulses.

20. (previously presented) The asynchronous pulse logic circuit of claim 19 further comprises:

an acknowledgment block comprising a second pulse generating component for generating a resetting pulse.

21. (previously presented) The asynchronous pulse logic circuit of claim 20 further comprises:

a conditions block whereby said second pulse generating component is controlled by said conditions block to conditionally reset each of said plurality of input-output blocks and input clearing block.

22. (previously presented) The asynchronous pulse logic circuit of claim 21 wherein said conditions block further comprises:

a third pulse generating component for generating a sending pulse; and

a third converting component for converting pulses to said first level voltage connected to said third pulse generating component

23. (currently amended) An asynchronous pulse logic circuit comprising:

a first pulse generating component for generating a sending pulse;

a first converting component for converting pulses to a first level voltage connected to said first pulse generating component wherein said first converting component is modified to store states; and

an updating component comprising an interlock component wherein an updating pulse is generated to update the input state in said first pulse generating component, whereby a state storing circuit is formed.

24. (previously presented) The asynchronous pulse generating circuit of claim 23 further comprises:

an arbiter-filter and

a checking component for ensuring no old output is still pending whereby said checking component and said arbiter-filter are connected to said first pulse generating component and said first converting component to form a STAPL arbiter.

25. (previously presented) The asynchronous pulse generating circuit of claim 24 wherein said first pulse generating component generates a reset pulse for the input.

26. (previously presented) The asynchronous pulse generating circuit of claim 24 wherein said first pulse generating component further comprises an interlock component.

27. (previously presented) The asynchronous pulse generating circuit of claim 16 further comprises:

a QDI buffer connected to said STAPL left-right buffer whereby an STAPL-to-QDI converter is formed.

28. (previously presented) The asynchronous pulse generating circuit of claim 16 further comprises:

a QDI buffer connected to said STAPL left-right buffer whereby an QDI-to-STAPL converter is formed.